Abstract of the Disclosure

An MOS device is formed comprising a semiconductor layer of a first conductivity type, a first source/drain region of a second conductivity type formed in the semiconductor layer, and a second source/drain region of the second conductivity type formed in the semiconductor layer and spaced apart from the first source/drain region. The MOS device further comprises a gate formed proximate an upper surface of the semiconductor layer and at least partially between the first and second source/drain regions, and a shielding structure formed proximate the upper surface of the semiconductor layer and between the gate and the second source/drain region, the shielding structure being electrically connected to the first source/drain region, the shielding structure being spaced laterally from the gate and being non-overlapping relative to the gate. In this manner, the MOS device is substantially compatible with a CMOS process technology.